Fig. 1

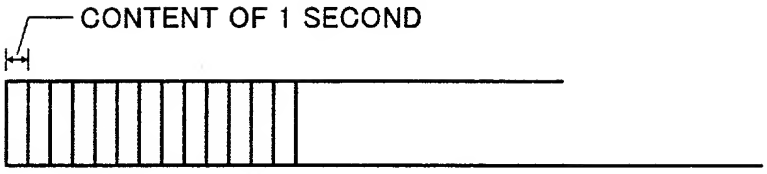

Fig. 2

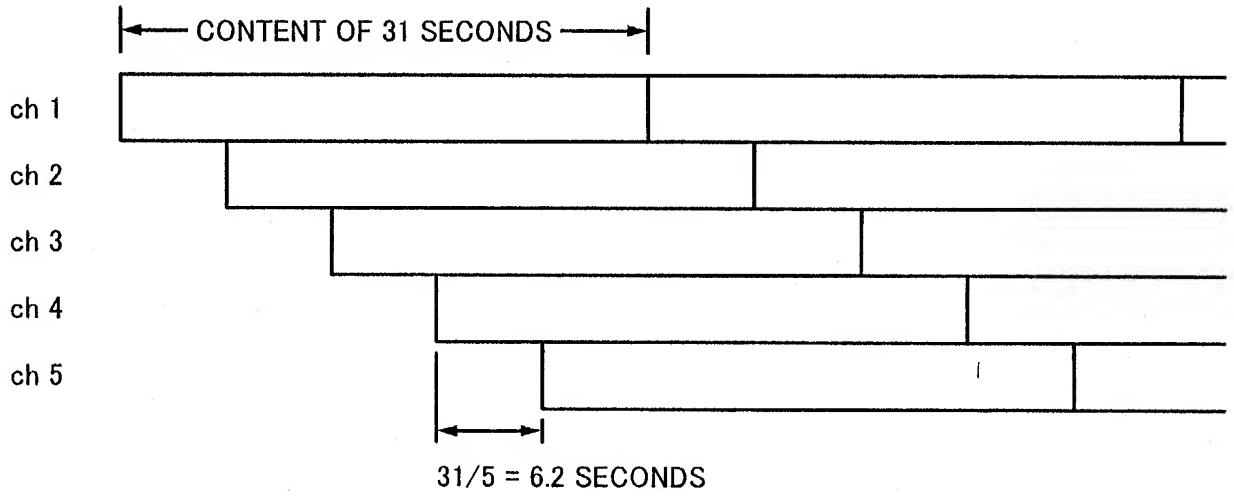

Fig. 3

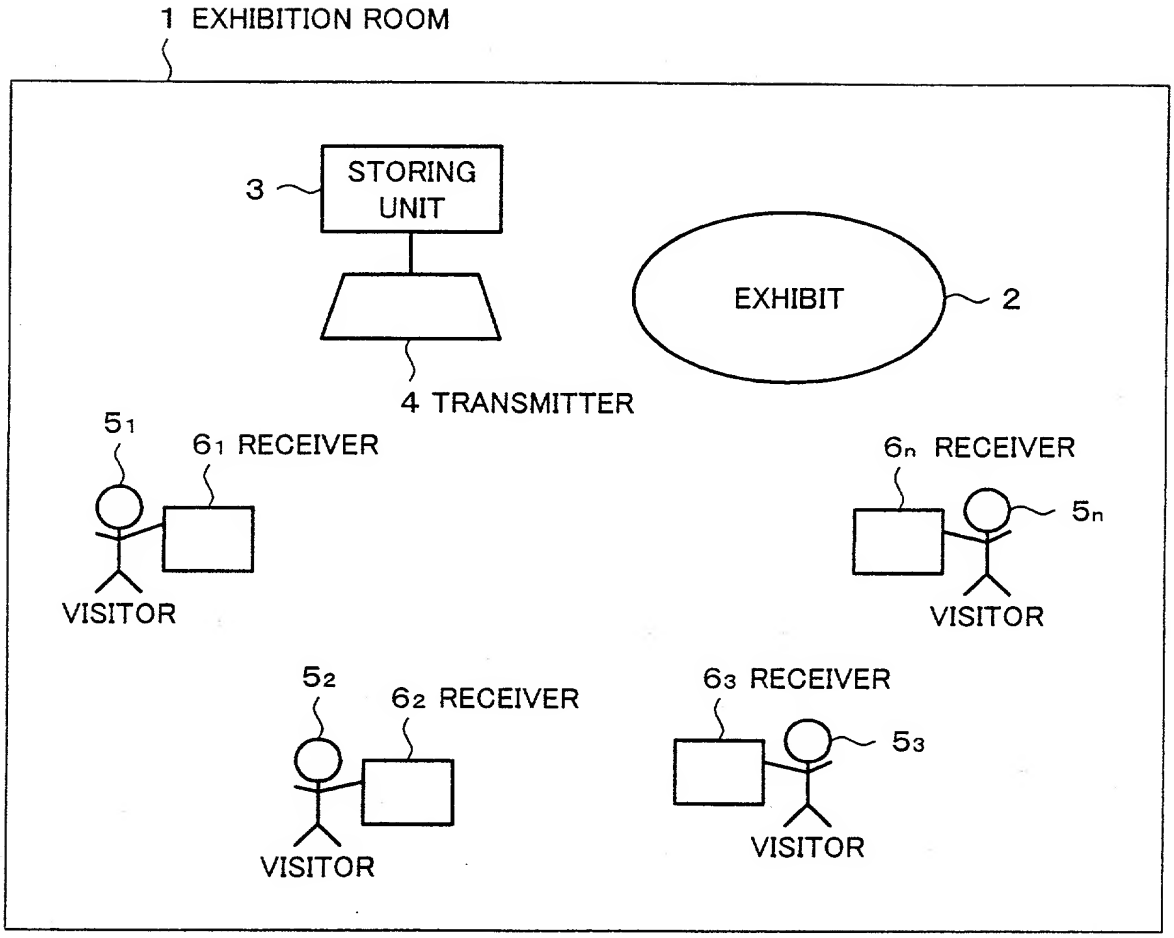
1 EXHIBITION ROOM
3
STORING UNIT
4 TRANSMITTER
EXHIBIT
2
5₁
6₁ RECEIVER
VISITOR
6n RECEIVER
5n
VISITOR
5₂
6₂ RECEIVER
VISITOR
6₃ RECEIVER
5₃
VISITOR

Fig. 4

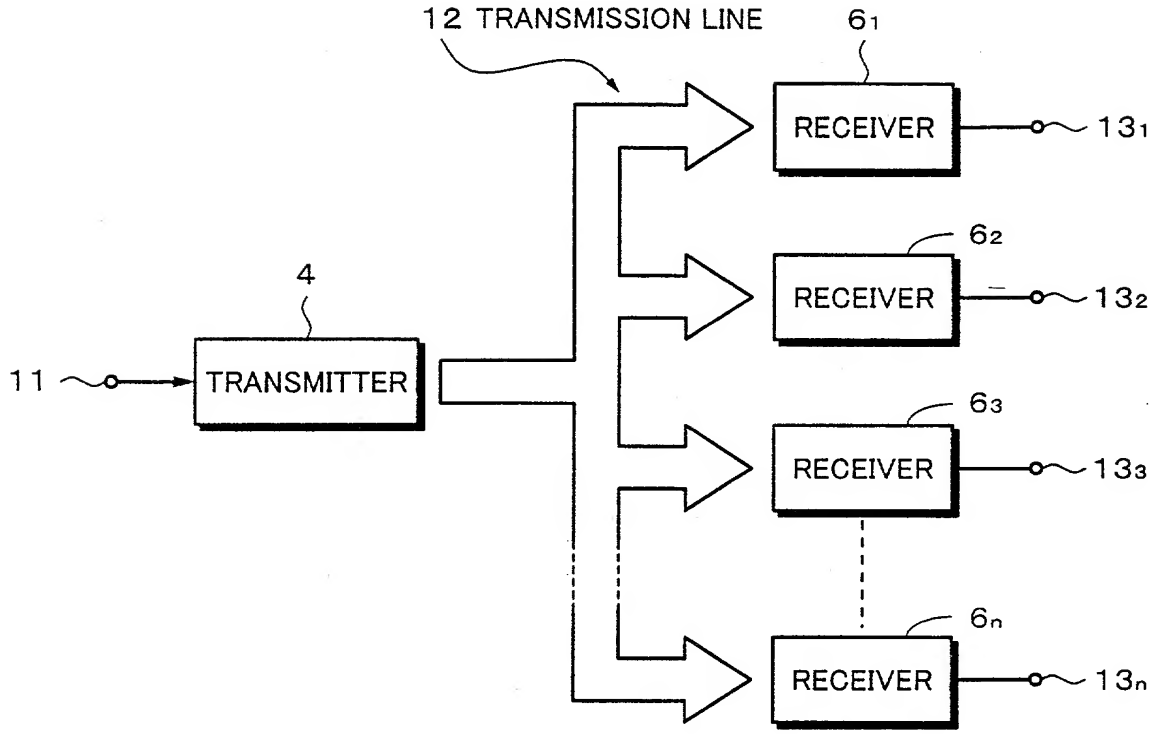

Fig. 5A

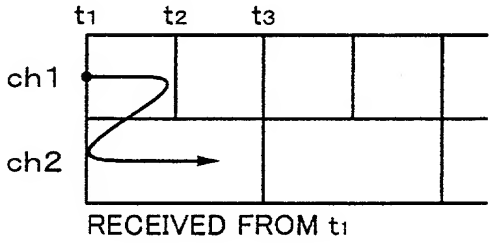

Fig. 5B

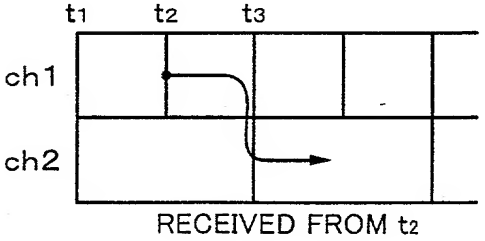

Fig. 6

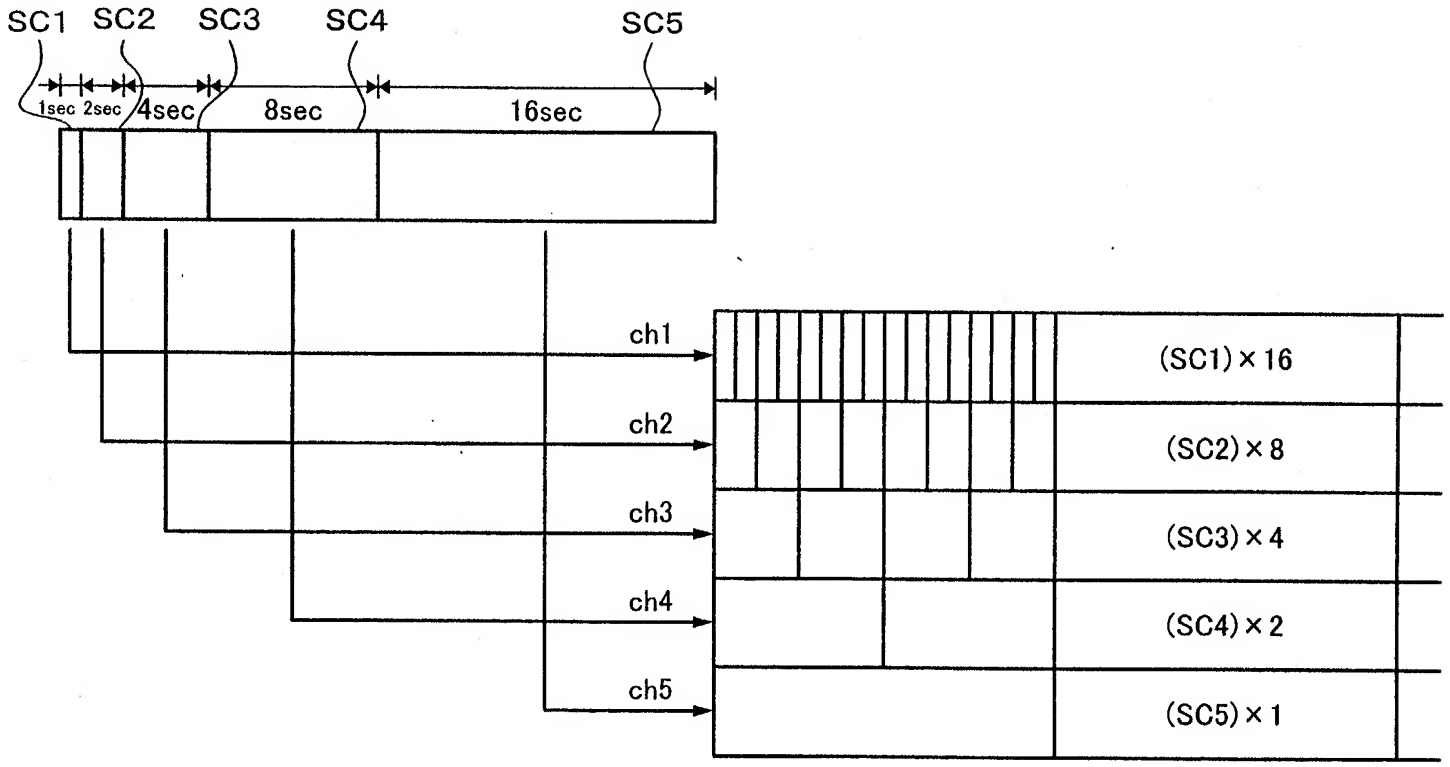
SC1
SC2
SC3
SC4
SC5
1sec
2sec
4sec
8sec
16sec
ch1
ch2
ch3
ch4
ch5
(SC1) × 16
(SC2) × 8
(SC3) × 4
(SC4) × 2
(SC5) × 1

Fig. 7

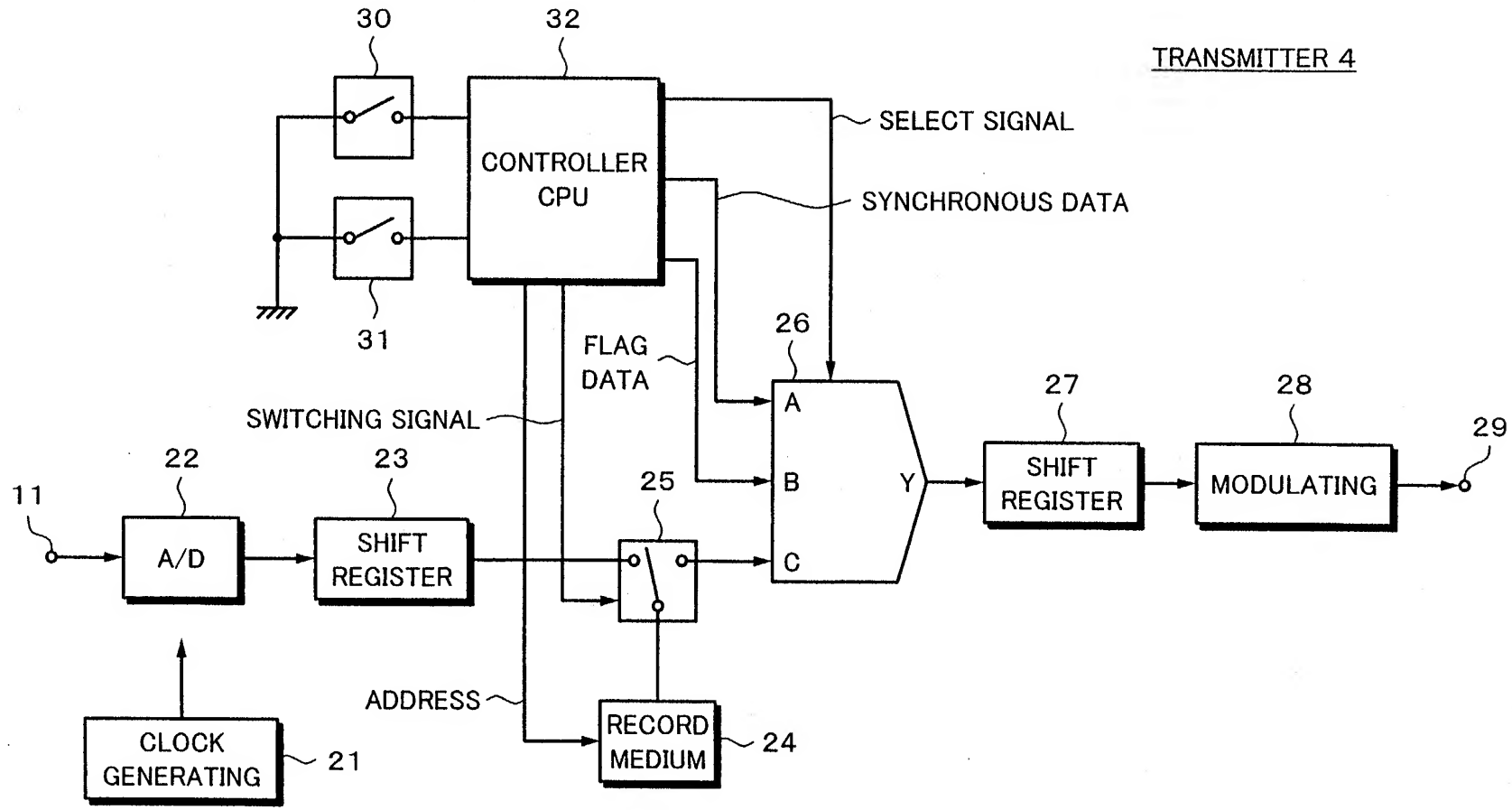
TRANSMITTER 4
30
32
CONTROLLER CPU
SELECT SIGNAL
SYNCHRONOUS DATA
31
FLAG DATA
26
SWITCHING SIGNAL
A
B
C
Y
27
28
29
SHIFT REGISTER
MODULATING
11
22
23
25
A/D
SHIFT REGISTER
ADDRESS
CLOCK GENERATING
21
RECORD MEDIUM
24

Fig. 8A

	ADDRESS
BSC1	0
BSC2	4E20
BSC3	EA60
BSC4	222E0
BSC5	493E0
BSC6	975E0
BSC7	1339E0

Fig. 8B

	ADDRESS
ESC1	4E1F
ESC2	EA5F
ESC3	222DF
ESC4	493DF
ESC5	975DF
ESC6	1339DF
ESC7	26C1DF

ARSC1
ARSC2
ARSC3
ARSC4
ARSC5
ARSC6
ARSC7

Fig. 9

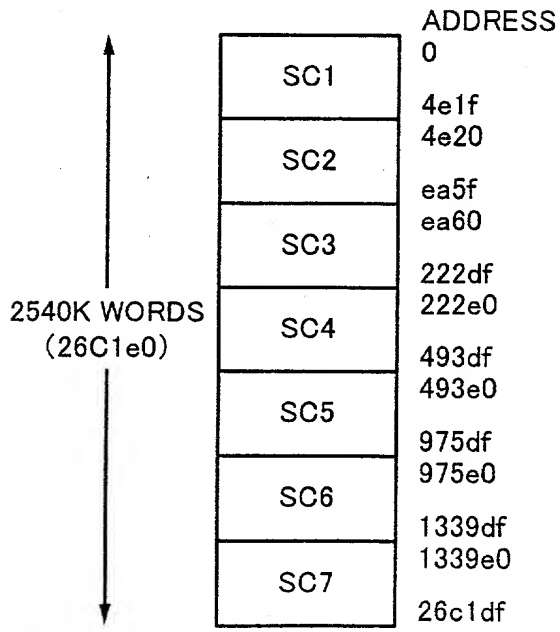

Fig. 10A

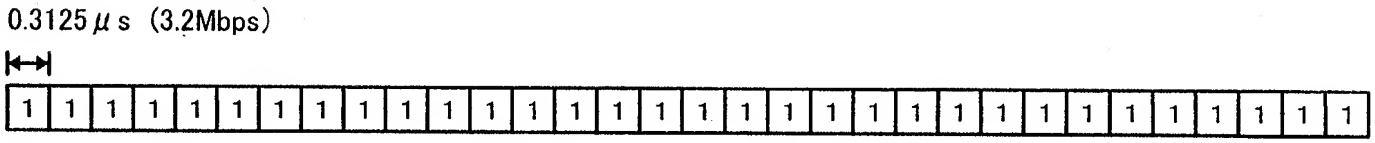

Fig. 10B

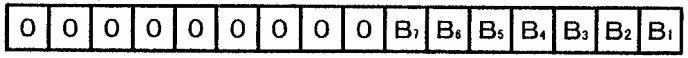

Fig. 10C

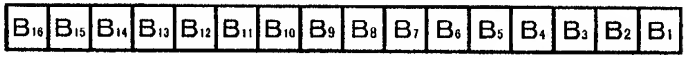

Fig. 11

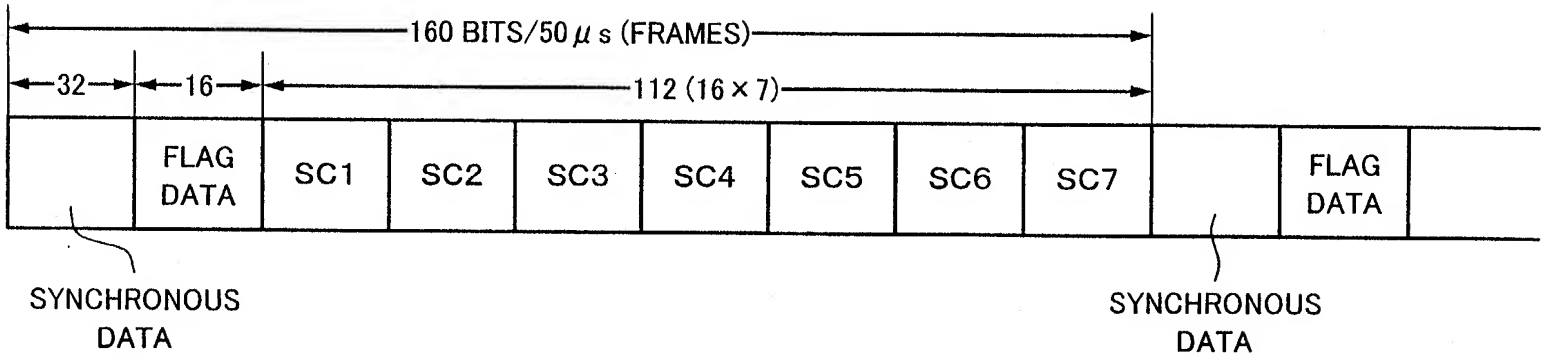
160 BITS/50 μ s (FRAMES)
32
16
112 (16 × 7)
FLAG DATA
SC1
SC2
SC3
SC4
SC5
SC6
SC7
FLAG DATA
SYNCHRONOUS DATA
SYNCHRONOUS DATA

Fig. 12

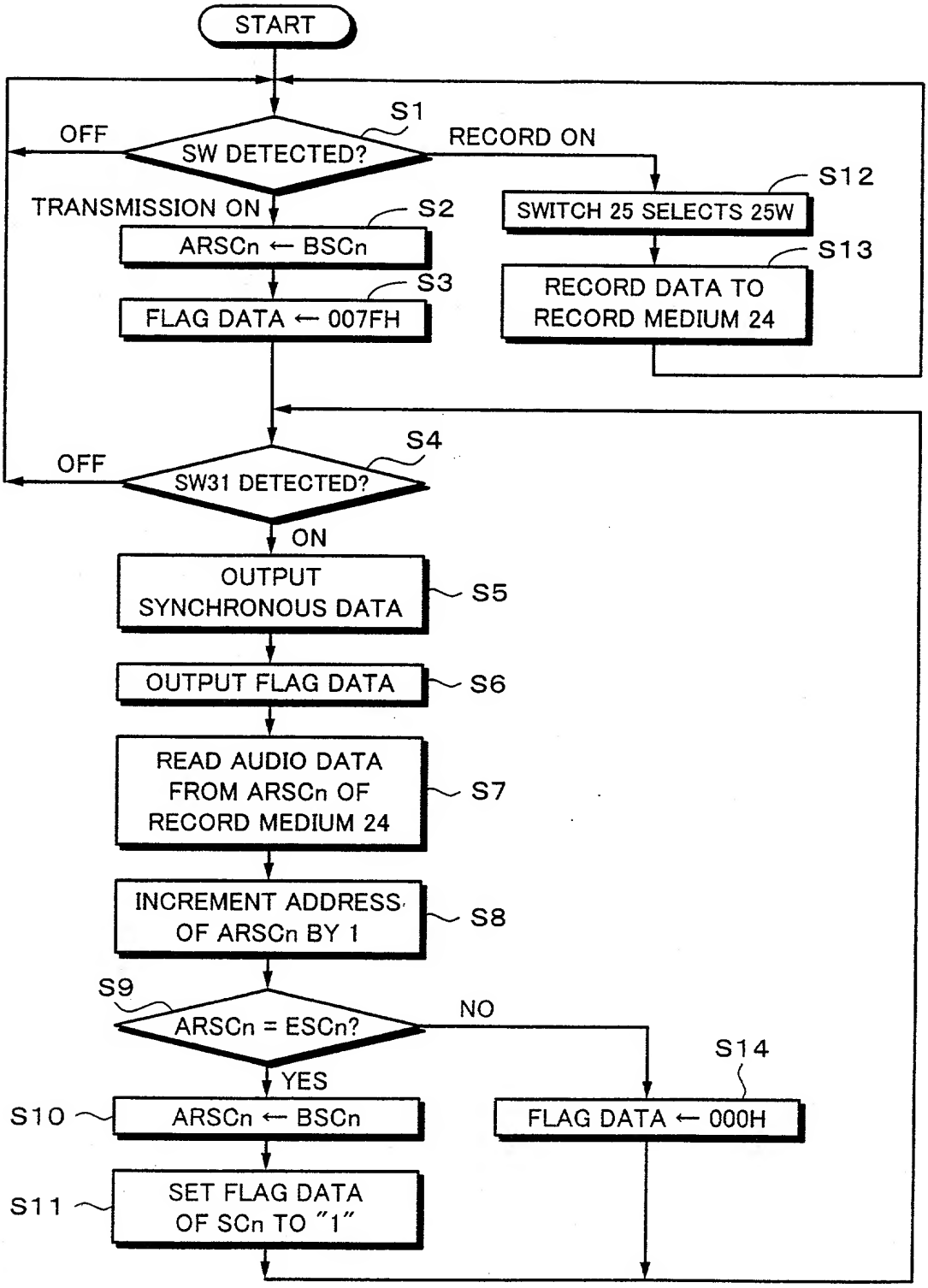
START
S1
SW DETECTED?
OFF
RECORD ON
TRANSMISSION ON
S2
ARSCn ← BSCn
S3
FLAG DATA ← 007FH
S12
SWITCH 25 SELECTS 25W
S13
RECORD DATA TO RECORD MEDIUM 24
S4
SW31 DETECTED?
OFF
ON
OUTPUT SYNCHRONOUS DATA
S5
OUTPUT FLAG DATA
S6
READ AUDIO DATA FROM ARSCn OF RECORD MEDIUM 24
S7
INCREMENT ADDRESS OF ARSCn BY 1
S8
S9
ARSCn = ESCn?
NO
YES
S14
FLAG DATA ← 000H
S10
ARSCn ← BSCn
S11
SET FLAG DATA OF SCn TO "1"

Fig. 13

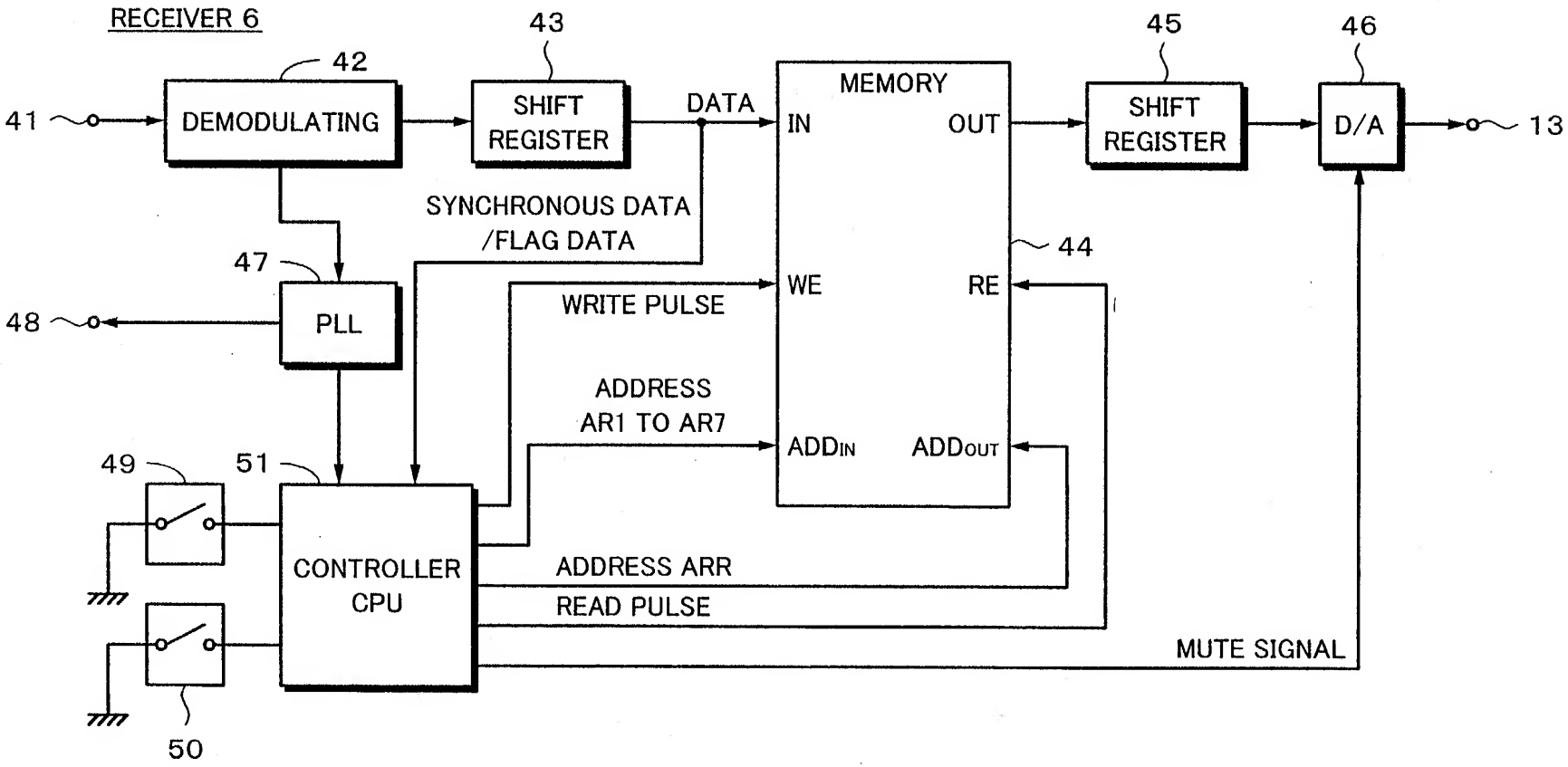
RECEIVER 6
41
42
DEMODULATING
43
SHIFT REGISTER
DATA
MEMORY
IN
OUT
45
SHIFT REGISTER
46
D/A
13
SYNCHRONOUS DATA /FLAG DATA
47
PLL
48
44
WE
RE
WRITE PULSE
ADDRESS AR1 TO AR7
ADDIN
ADDOUT
49
51
CONTROLLER CPU
ADDRESS ARR
READ PULSE
MUTE SIGNAL
50

Fig. 14A

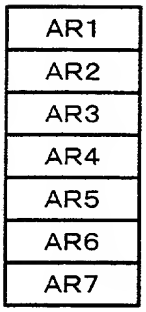

Fig. 14B

Fig. 14C

Fig. 14D

Fig. 14E

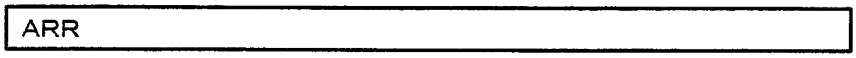

Fig. 15A

Fig. 15

Fig. 15A

Fig. 15B

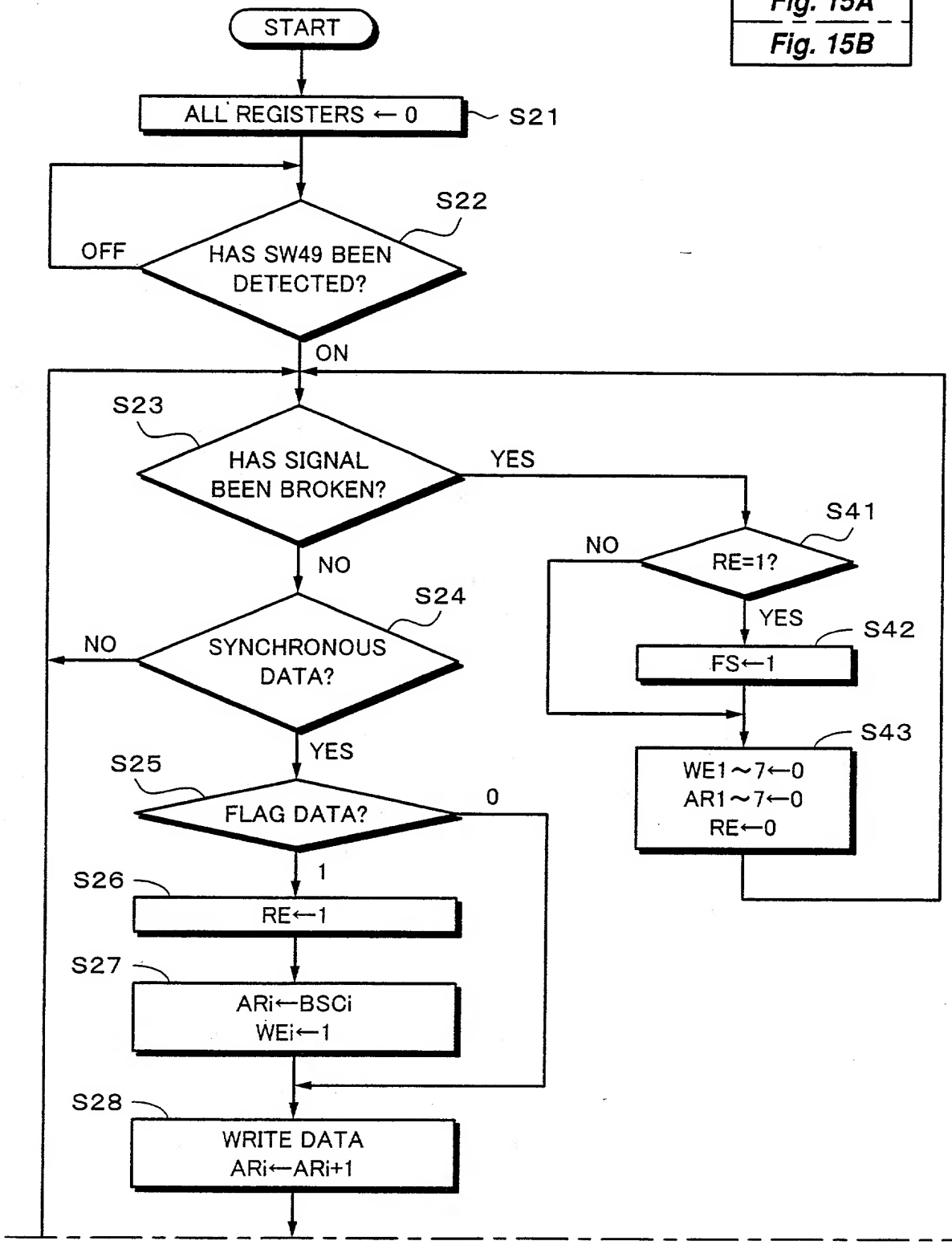

Fig. 15B

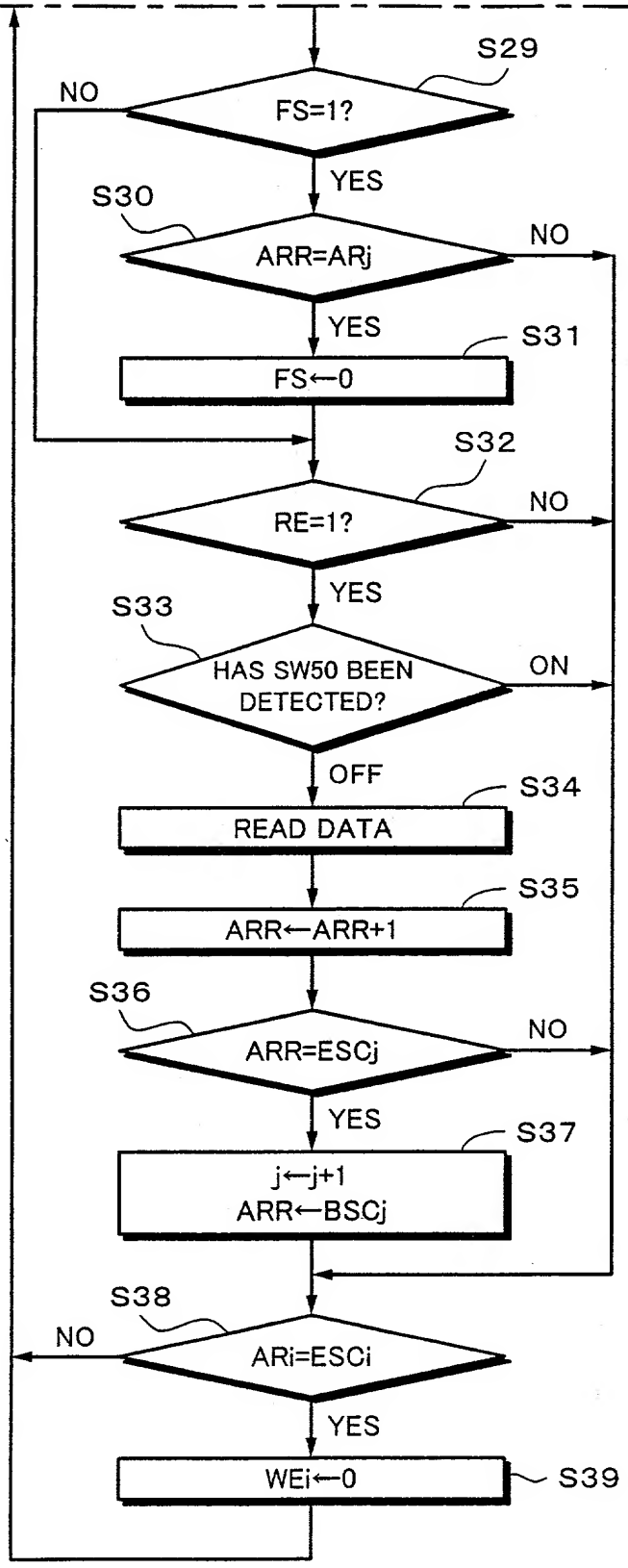
S29
FS=1?
NO
YES
S30
ARR=ARj
NO
YES
S31
FS←0
S32
RE=1?
NO
YES
S33
HAS SW50 BEEN DETECTED?
ON
OFF
S34
READ DATA
S35
ARR←ARR+1
S36
ARR=ESCj
NO
YES
S37
j←j+1
ARR←BSCj
S38
ARi=ESCi
NO
YES
WEi←0
S39

Fig. 16

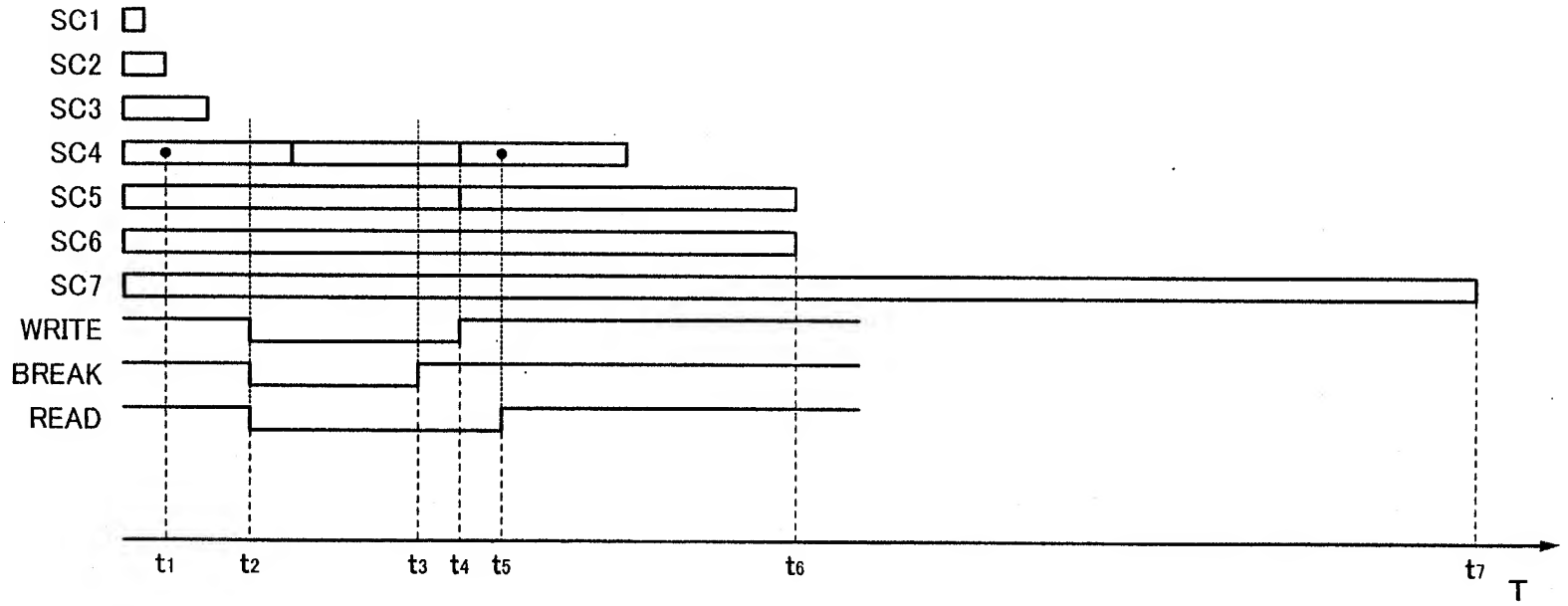

Fig. 17

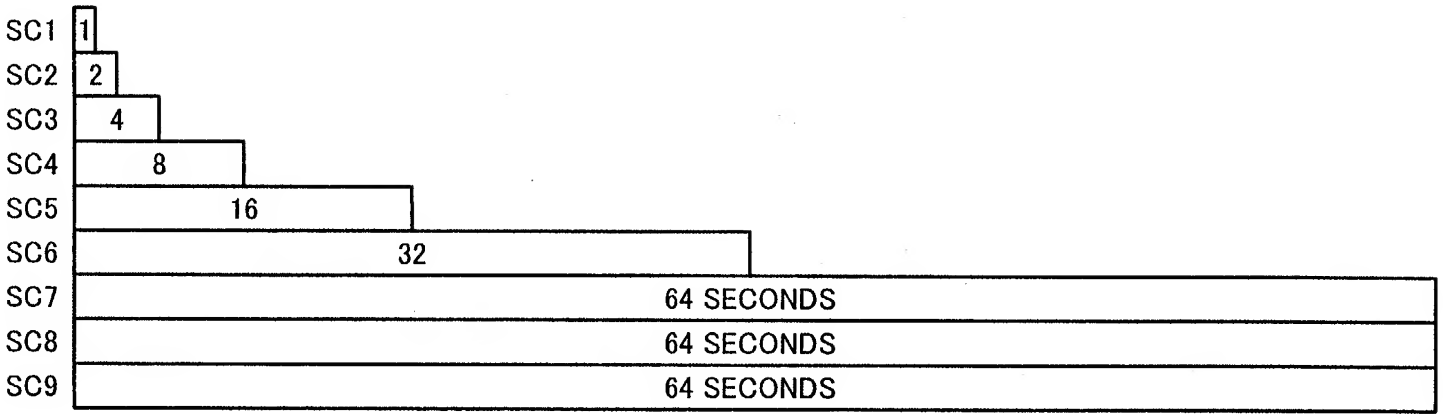
SC1
1
SC2
2
SC3
4
SC4
8
SC5
16
SC6
32
SC7
64 SECONDS
SC8
64 SECONDS
SC9
64 SECONDS

Fig. 18

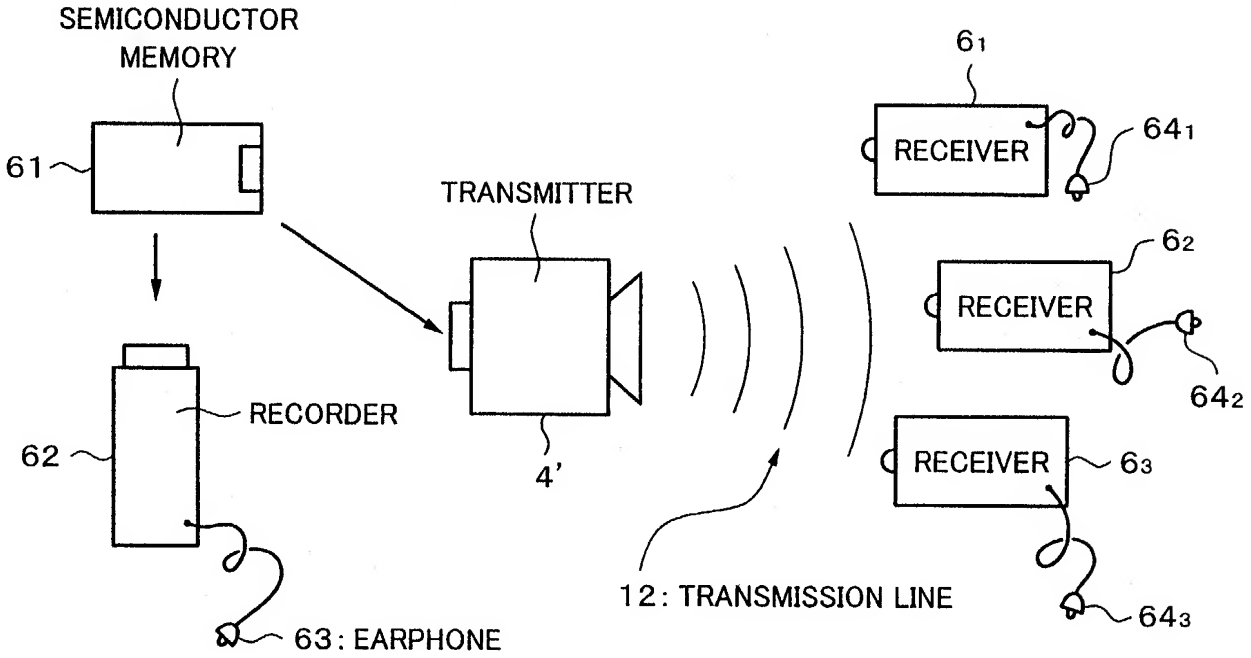

Fig. 19A

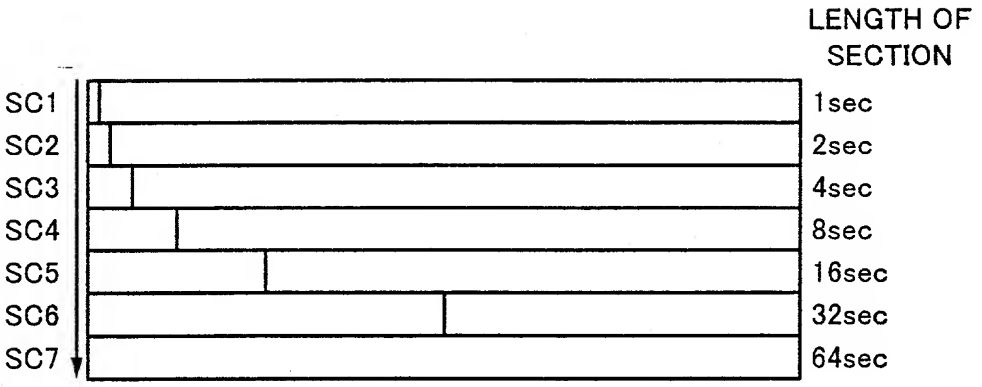

Fig. 19B

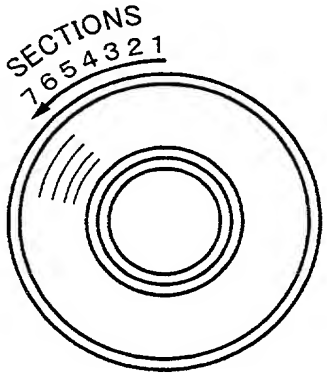

Fig. 19C

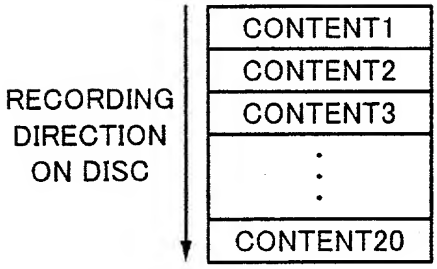

Fig. 19D

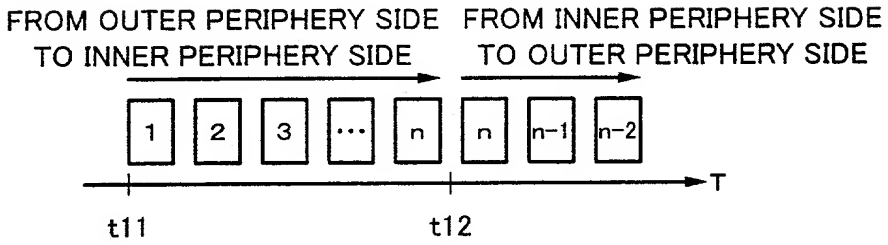

Fig. 20

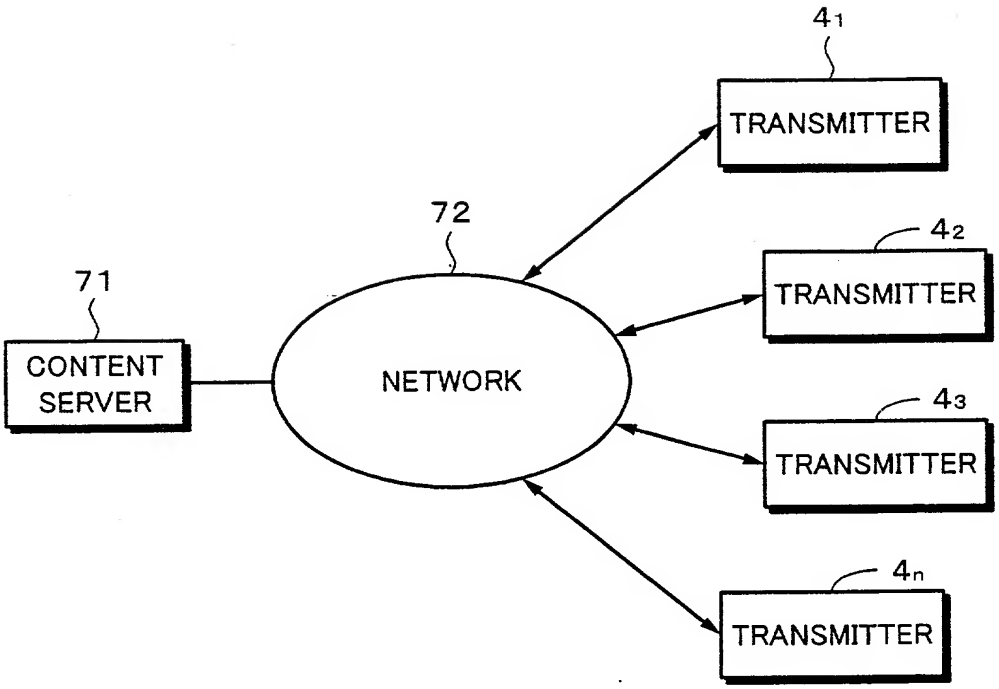
41
TRANSMITTER
72
42
TRANSMITTER
71
CONTENT SERVER
NETWORK
43
TRANSMITTER
4n
TRANSMITTER

Fig. 21

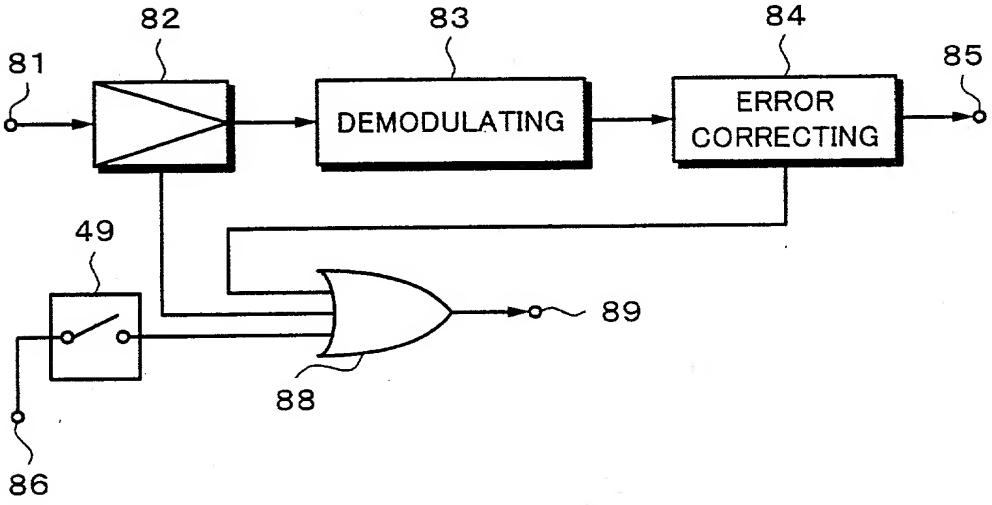
82
83
84
81
85
DEMODULATING
ERROR CORRECTING
49
89
88
86

Fig. 22A

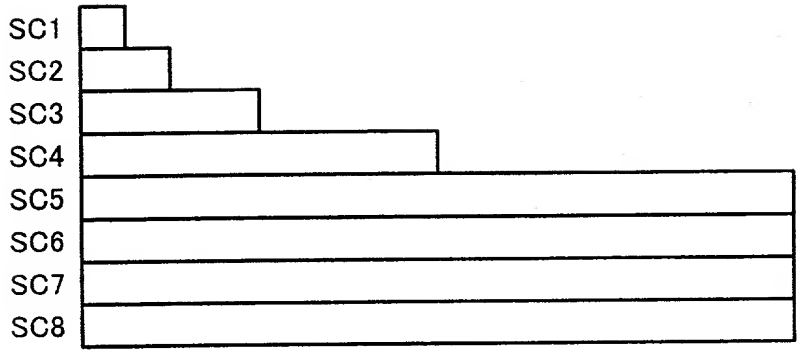

Fig. 22B

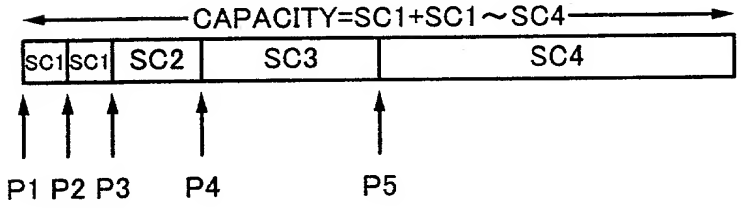

Fig. 23A

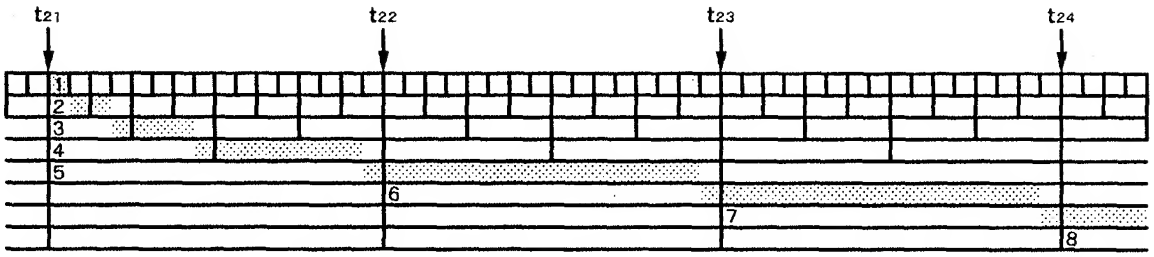

Fig. 23B

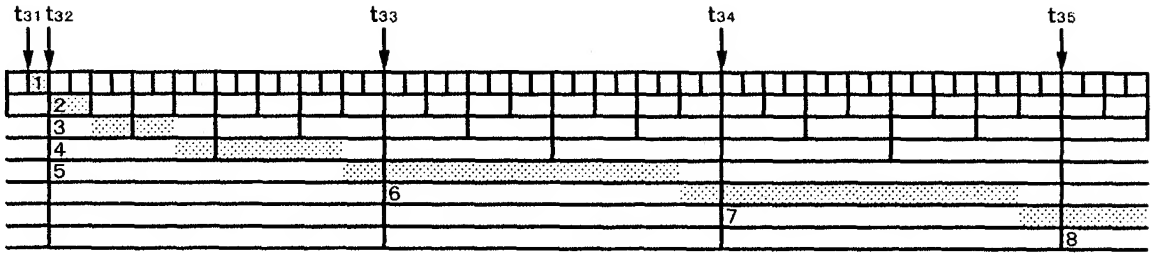

Fig. 23C